A Study of High-Performance Frequency Synthesizer Based on Digital Bang-Bang Phase-Locked Loop for Wireless Applications

Doctoral Dissertation of: Tuan Minh VO

Advisor: Prof. Salvatore LEVANTINO
Tutor: Prof. Ivan RECH
Supervisor of the Doctoral Program: Prof. Barbara PERNICI

2019-XXX
Introduction

High-performance frequency synthesizer is a fundamental part of almost any modern wireless communication device, for example, used for coherent demodulation/modulation in wireless transceivers. The frequency synthesizer based on phase-locked loop (PLL) architecture, serving as a local oscillator in a transceiver, is indeed a negative feedback control system generating an output signal whose frequency is multiple of the reference signal frequency. The multiple can be an integer or a fractional number. Though fractional-$N$ PLLs entail the key advantage of a finer frequency resolution, the noise-power figure-of-merit (FoM) of state-of-the-art integer-$N$ PLLs is still better than in the fractional-$N$ case. In addition, digital PLL synthesizers are taking over conventional analog ones, because of their benefits in terms of power consumption and area occupation in ultra-scaled CMOS technologies. The digital solution simplifies the design and, as this is portable to the next technology nodes, may potentially reduce the time-to-market. In this study, a type-II fractional-$N$ digital PLL having a phase detector (PD) with only two output levels of 1 and −1 is of interest. Though this topology of fractional-$N$ digital PLL has been demonstrated in practice being able to obtain a FoM close to the best of the integer-$N$ ones, there is a lack of theoretical literature that explains in detail the adopted techniques in the system.

It is known that the one-bit (also known as bang-bang, BB) phase detector, when employed in frequency synthesizers, only acts like a linear element when phase (time) error at the PD input is dominated by random noise. Since the quantization noise of the digital ΔΣ modulator (DSM) dithering the modulus control of the frequency divider is not white and much larger than other thermal random noise in the system, this noise may cause a limit cycle in the BB-PLLS. To address this issue, a digital/time converter (DTC) is placed in the feedback path between the divider and the BBPD. The control gain of the DTC is automatically adjusted in background by a calibration loop operating based on the principle of the least-mean-square (LMS) adaptive filter. The calibration loop helps the PLL to adapt to changes in the digitally-controlled oscillator (DCO) period as well as the DTC characteristics in practice. By far, in the presented publications, to guarantee a short convergence time, an at least second-order DSM is required when a fine frequency resolution is desired. This follows a large DTC range of twice of the DCO period in the system and this compromises jitter performance. In addition to the issue related to the quantization noise, the BB-PLLS also face an extremely long transient process when a large jump of the output frequency is required. Indeed, the frequency locking time of the BB-PLLs is shown to be inversely proportional to the values of the loop filter gains while these gains are very small to guarantee the loop stability. To solve the problem, a frequency-aid technique has been proposed. This technique is essentially based on exploiting digital ternary phase detectors (TPDs) to create multi filters in the feed-forward path of the BB-PLL. The outputs of the filters are used to tune a multi-bank DCO in corresponding order. The frequency-aid circuit is only triggered...
when the time error at the BBPD input is larger than a fixed value, i.e. the dead-zone of the TPD. In the published report, the lower bound of the dead-zone is large which may not be optimum for the frequency locking time. Furthermore, even when this technique is adopted, the frequency locking transient in the conventional system still requires relatively long time in cases the DCO tuning words are at their worst conditions.

The objective of this thesis is firstly to give an insight, for the first time, into the behavior during the transient of the fractional-N digital BB-PLL in two separated cases, i.e., with the frequency aid technique in the first case and with the LMS calibration loop in the second one. In order to reach this goal, analysis is carried on in the time domain for the frequency aid technique. Based on the analyzed result, we propose a novel frequency aid technique to further improve the frequency locking speed. In the worst case of the frequency locking, the proposed technique reduces the transient time by a factor of 3.5. The LMS calibration loop is evaluated in accordance to the value of the fractional part of the frequency control word \( f_{cw} \). The analysis, that is carried on in both the time-domain and the z-domain, not only gives the qualitative results but also quantity results in some particular cases. Moreover, two novel calibration schemes are proposed in order to use a smaller delay range DTC while keeping a short convergence time. At the same convergence time, the required DTC time range in the first proposed scheme is 0.57 times, and, the one in the second proposed scheme is 0.55 times as of the one in the conventional schemes, respectively. All the analysis are verified by simulation based on accurate behavioral models. The models are built with real design parameters, and, designed for BB-PLLs synthesizing an output frequency from 3.2 GHz to 4.0 GHz from a reference frequency of 52 MHz.

This Ph.D. dissertation is organized as follows.

Chapter 1 firstly make a review of the typical structure of a \( \Delta \Sigma \) fractional-N digital PLL. The functions as well as the models for simulation of the main blocks that are used throughout the thesis are mentioned. The first part of the chapter shows that for the digital PLLs, the bottleneck is represented by the multi-bit time to digital converter (TDC), which acts as a phase detector. In the latter, a solution using a single bit TDC is reported. This type of TDC helps to break the trade-off between the time resolution and power consumption, and leads to a better jitter noise-power consumption FoM for a digital PLL. The operating principle and the issues in the realization of the fractional-N digital BB-PLLs are explained in detail. To address the issue, this chapter also presents the solution of exploiting a DTC to make a true fractional divider. Furthermore, the common topologies of the DTC are introduced.

In chapter 2, the frequency aid technique that is used to improve the transient time of the BB-PLL is presented. Because the frequency aid circuit is activated during the frequency locking process, the study of this technique is carried on based on a non-linear model. Due to the overlap of frequency range between the banks of the DCO, the behavior of the time error at the BBPD input in general can be divided into three stages when the frequency aid circuit is activated. Among them, the second stage usually needs the longest time to finish because of the unstable state of the tuning word of the DCO coarse bank. To solve this problem, in the end of the chapter, our study proposes an enhanced frequency aid technique by placing a digital monitor to recognize the timing that the tuning word of the coarse bank should be fixed. Thanks to the proposed technique, the process of jumping back and forth between two adjacent levels of the coarse bank tuning word is dismissed. Hence, the frequency locking
needs a less sampling clock to reach the steady state.

**Chapter 3** is devoted for the analysis of the LMS calibration loop. By expressing the BBPD with a linear block in the random noise regime of the BB-PLL, it is possible to evaluate the variance of the LMS gain fluctuation. Basically, in this regime, the power of the gain is decided by its frequency response to the thermal random noise being dominant at the BBPD input. Moreover, we make a review of the digital DSM, which is necessary for all fractional-\(N\) digital \(\Delta\Sigma\) PLLs, based on the Multi-stAge noise SHaping (MASH) structure. In our study, a mathematical error-feedback model adopting the multi-bit quantizer is used. By computing the dynamic range of the quantization noise, it is shown that the required delay range of the DTC depends exponentially on the order of the DSM. In addition, the waveform of the accumulated quantization error induced by the DSM with a constant input is analyzed as well. To the best of the author’s knowledge, a similar analysis for the second-order DSM has never been appeared in literatures so far. Along with the non-linear model, such waveform lays the foundations to explain the convergence process of the LMS gain, in particular, versus the value of the \(f_{cw}\) fractional part. In practice, error issued in the DTC may include the gain error caused by change of the DCO period and the non-linearity error caused by the process, voltage and temperature (PVT) mismatches. Therefore, at the last part of this chapter, a digital piecewise-linear pre-distortion technique with multi LMS gains to calibrate these error in the DTC is introduced. In essence, the time error injected into the BB-PLL by the DSM quantization noise is divided into evenly piecewises, each piece is cancelled out by a specific part of the DTC. Intuitively, to select the proper part of the DTC, a pair of adaptive gains is needed in every sampling cycle, namely, one gain is used to cancel out the gain error while the another one is used to cancel out the non-linearity error.

**Chapter 4** proposes a novel segmented scheme for the DTC aiming to relax the trade-off between the LMS convergence time versus the DTC delay range. The novel scheme is built by placing a dithering block between the \(f_{cw}\) and the first-order DSM controlling the divider. Thanks to this structure, more abrupt steps are generated in one iteration of the accumulated quantization error. At the same time, because the noise added by the dithering block is divided by a factor much larger than 1, the required time range of the DTC to cancel out this noise is small. Consequently, the adaptive gain can be updated with a fast speed while the range of the DTC is still kept in a allowable range. Furthermore, the multiplication factor adopted in this scheme allows the designers choosing the optimum solution for the mentioned trade-off depending on the application.

In **Chapter 5**, another novel calibration loop scheme is proposed. However, this scheme is more suitable for the phase interpolator (PhI)-DTC hybrid structure. The key idea of the proposed scheme is to use both the PhI and the DTC to cancel out the time error injected by the training sequence of the LMS calibration loop instead of using only the DTC as in the conventional scheme. To realize this, an additional quantizer with pre-defined threshold values is placed at the output of the LMS calibration loop. So, the DTC is needed to cancel out only the residue of the additional quantizer while the waveform of the training sequence of the LMS loop is unchanged. By this way, the convergence of the adaptive gain is guaranteed in a short time while the range of the DTC is reduced in compared with the conventional scheme. Despite the fact that, one more calibration loop is needed to compensate the mismatch between the pre-defined threshold values and the real ones, the error of the new gain is so small that its convergence time is not considerable.
In summary, the original contributions of the thesis are: a novel frequency aid technique (not published yet); a detailed explanation to the convergence and the noise of the LMS calibration loop (not published yet); and, two novel schemes for the DTC calibration loops. The results of study have been published in three articles on international conferences.


**Abstract** The adoption of the digital/time converter (DTC) circuit in fractional-N phase-locked loops (PLLs) allows the realization of high-performance bang-bang digital PLLs suitable for wireless communications. In this paper, a general expression of the dynamic range required for the DTC is derived as a function of the order of the Delta-Sigma modulator driving the frequency-divider module. Based on this, it is shown how the combination of the DTC with the M-phase switching technique helps to relax the DTC dynamic range by a factor of M and reduce its nonlinearity. The effectiveness of the phase switching technique is demonstrated via behavioral-level simulation of a digital PLL in the case of first-, second-, and third-order Delta-Sigma modulator.


**Abstract** The adoption of the digital/time converter (DTC) circuit has improved the performance of ΔΣ fractional-N phase locked loops (PLLs). Accurate cancellation of ΔΣ quantization error via the DTC requires an automatic calibration made by an LMS loop. A high-order ΔΣ speeds up calibration convergence and improves PLL spectral purity, though at the price of larger quantization error and wider DTC range. To overcome this problem, we propose an innovative parallel segmentation scheme which reduces the range of quantization error without compromising spectral purity and convergence speed. The effectiveness of the proposed segmentation scheme is demonstrated via behavioral-level simulations of a digital PLL and compared to the conventional cascaded segmentation scheme.


**Abstract** In today’s fractional-N phase-locked loops, digital-to-time converters are commonly used to cancel the quantization noise of the divider module, and a least-mean squares loop is used to adapt the gain of the cancellation path. Unfortunately, a trade-off exists between the time range needed to the digital-to-time converter and the speed of convergence of the calibration. In this paper, a novel scheme significantly relaxing this trade-off and allowing for a low-power implementation of both the digital-to-time converter and the calibration loop, is introduced. The effectiveness of the proposed concept is verified via behavioral simulations in the presence of circuits non-idealities, showing a reduction of at least a factor of 5x in the settling time of the calibrated coefficient.
Acknowledgments

I would like to acknowledge many people for helping me during my doctoral work at Politecnico di Milano, Italy.

First and foremost I would like to express my sincere thanks and appreciation to my PhD thesis supervisor, Professor Salvatore Levantino. He gave me a chance to do the doctoral work in the field of RF integrated circuit design although my experience in this field was so little. He has supported me with many thing not only in the study but also other thing during my time in Italy. Thank you for your patience and understanding. I will always remember it. Hope we still have chance to work together in the future after I come back Vietnam.

I am also grateful to Professor Carlo Samori, for his involvement and continued support to my research. I am greatly thankful to Professor Andrea Leonardo Lacaita, for having shared so much of his time and insight during our many discussions. His suggestions have been particularly constructive and have contributed greatly to my study. It is really my pleasure to work with all of you.

I thank my committee, Professor Kenichi Okada, Tokyo Institute of Technology, Japan and Professor Pietro Andreani, University of Lund, Sweden for their precious time and commitment.

I thank to many people in our Lab: Luigi, Dmytro, Domenico, Truppi, Garghetti, Mario, Santiccioli, Stefano, Tang, for their discussion about the research as well as daily life conversations. I have learned many thing from them. Special thank to Luca, who helped me with many technical problems and when my daughter was born in Milan.

I would like to thank very much to Ms. Elena Cortiana, Ms. Francesca Clemenza and Ms. Rosa Alba Petrelli, for supporting a foreigner student like me a lot with the paper work from the beginning of the PhD course until now. Many thanks to the DEIB and Polimi, for the support. I am proud to be one of the graduated student from here.

I also thank to many of my friends and my roommates: Thai, Vy, Calo, Vinh, Thanh, Quan, Lam, Quang, Van Anh who helped me and enjoyed with me life in Italy. Many thanks to Dr. Dao Le Anh, Ng. Th. Bich Nguyen, Dr. Phan Thanh Nhan, Thao, Danh, Linh who shared with me the happiness as well as the sadness when I was alone in Italy. I had a lot of fun with them and it helped me a lot to overcome many stressful thing.

I also want to gratefully acknowledge the scholarship under the Project 911 from Vietnamese Government, for the financial support during my doctoral work.

Last but not least, thanks my family from the bottom of my heart. I would like to thank my parents Vo Xuan Tien and Hoang Thi Ha for being the best parents who always support me with everything, make me feel peaceful all the time, and my brother Vo Hoang Minh for his support. I would like to thank all members of my wife family for taking care of my wife and my daughter during the time I was not in Vietnam. To my lovely wife Truong Cong Vu Hlang and my 3.5 year-old daughter Vo Khanh Linh, thank you for your love, support and encouragement during all the years I have spent in PhD research. It was really difficult to live apart for such a long time but you did overcome. For me, it was truly hard to look after a baby alone, it feels like more stressful than doing a PhD research. I love you very much.
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<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>$BW_{pl}$</td>
<td>PLL closed-loop bandwidth.</td>
</tr>
<tr>
<td>$c$</td>
<td>Carry of the quantizer.</td>
</tr>
<tr>
<td>$cw$</td>
<td>DTC control word.</td>
</tr>
<tr>
<td>$D_{pl}$</td>
<td>Number of clock delays at the loop filter.</td>
</tr>
<tr>
<td>$E_n$</td>
<td>Binary quantization error at the $n$-th stage quantizer.</td>
</tr>
<tr>
<td>$e$</td>
<td>BBPD output.</td>
</tr>
<tr>
<td>$e_1$</td>
<td>TPD output.</td>
</tr>
<tr>
<td>$F_r$</td>
<td>Frequency of the reference clock.</td>
</tr>
<tr>
<td>$f_d$</td>
<td>Frequency of the DCO.</td>
</tr>
<tr>
<td>$f_z$</td>
<td>Frequency of the zero of the PLL.</td>
</tr>
<tr>
<td>$fcw$</td>
<td>Frequency control word.</td>
</tr>
<tr>
<td>$G_{loop}$</td>
<td>PLL open loop gain.</td>
</tr>
<tr>
<td>$i$</td>
<td>Index of the pre-distortion gains.</td>
</tr>
<tr>
<td>$K_T$</td>
<td>Sensitivity of the general DCO period.</td>
</tr>
<tr>
<td>$K_{T0}$</td>
<td>Sensitivity of the DCO fine bank in time.</td>
</tr>
<tr>
<td>$K_{T1}$</td>
<td>Sensitivity of the DCO coarse bank in time.</td>
</tr>
<tr>
<td>$K_{bb}$</td>
<td>BBPD linearized gain.</td>
</tr>
<tr>
<td>$k$</td>
<td>Index at the reference sampling clock.</td>
</tr>
<tr>
<td>$k_d$</td>
<td>Index at the DCO clock.</td>
</tr>
<tr>
<td>$L$</td>
<td>Modulo of the $\Delta\Sigma$ modulator.</td>
</tr>
<tr>
<td>$\mathcal{L}$</td>
<td>Single-sided spectral density.</td>
</tr>
<tr>
<td>$LSB_c$</td>
<td>Resolution of the coarse DTC.</td>
</tr>
<tr>
<td>$M, M_p$</td>
<td>Multiplication factor.</td>
</tr>
<tr>
<td>$m, p, l$</td>
<td>Number of bit.</td>
</tr>
<tr>
<td>$mc$</td>
<td>Divider modulus control.</td>
</tr>
<tr>
<td>$N$</td>
<td>Division ratio.</td>
</tr>
<tr>
<td>$N_i$</td>
<td>Integer part of the division ratio.</td>
</tr>
<tr>
<td>$N_f$</td>
<td>Fractional part of the division ratio.</td>
</tr>
<tr>
<td>$n$</td>
<td>$\Delta\Sigma$ modulator order.</td>
</tr>
<tr>
<td>$n_g$</td>
<td>Number of gain in the pre-distortion technique.</td>
</tr>
<tr>
<td>$P$</td>
<td>Number of output level of multi-bit quantizer.</td>
</tr>
<tr>
<td>$P_{pl}$</td>
<td>PLL power consumption.</td>
</tr>
<tr>
<td>$Q_T$</td>
<td>Quantizer threshold value.</td>
</tr>
<tr>
<td>$Q_s$</td>
<td>Ratio of $\Delta t_{pl}/\Delta t_{dce}$.</td>
</tr>
<tr>
<td>$q, q_0, q_1, q_p$</td>
<td>Quantization error.</td>
</tr>
</tbody>
</table>
Symbols

\( q_{pp} \) Range of \( q \).
\( T_d \) Period of the DCO.
\( T_{dco} \) DTC time range.
\( T_{fb} \) Period of the feedback signal.
\( T_{frac} \) Time delay generated by the DTC.
\( T_r \) Period of the reference clock.
\( T_{d0} \) Period of the free-running DCO.
\( t_d \) Time stamp of the positive edges of the DCO output.
\( t_{div} \) Time stamp of the positive edges of the divider output.
\( t_{fb} \) Time stamp of the positive edges of the feedback signal.
\( t_r \) Time stamp of the positive edges of the reference signal.
\( t_w \) Tuning word of the DCO.
\( R \) Ratio of \( \alpha/\beta \).
\( r \) Residue of the quantizer.
\( s \) Thermal random noise.
\( w, w_0, w_1, w_p \) Accumulated quantization error.
\( w_{pp} \) Range of \( w \).
\( X_f \) Fractional part in integer number.
\( Y \) DSM output.
\( \alpha, \alpha_1 \) Loop filter integral path coefficient.
\( \beta, \beta_1 \) Loop filter proportional path coefficient.
\( \Delta f \) Frequency offset.
\( \Delta f_d \) Frequency resolution of the DCO.
\( \Delta f_{d1} \) Frequency resolution of the DCO coarse bank.
\( \Delta f_{d0} \) Frequency resolution of the DCO fine bank.
\( \Delta T \) Period offset.
\( \Delta T_{fr} \) Period error.
\( \Delta t \) Time error at the BBPD input.
\( \Delta t_{tdc} \) TDC resolution.
\( \Delta t_{phi} \) PHI resolution.
\( \Delta t_{d_2} \) Dead-zone of the TPD.
\( \epsilon, \epsilon_h, \epsilon_g \) Adaptive gain errors.
\( \gamma_1, \gamma_1, \gamma_2 \) Convergence factor.
\( \gamma_h, \gamma_g \) Convergence factor of the gain \( \hat{h}_i, \hat{g}_i \).
\( \hat{h}_1, \hat{h}_2 \) Gain of the LMS algorithm.
\( \hat{h}_i, \hat{g}_i \) Gains of the pre-distortion technique.
\( \hat{h}_{exp} \) Expected value of the LMS gain.
\( \hat{h}_{i,exp}, \hat{g}_{i,exp} \) Expected values of the pre-distortion gains.
\( \lambda_1 \) Frequency aid technique proportional path coefficient.
\( \psi \) Summation of the integral path.
\( \sigma_d \) PLL absolute jitter variance.
\( \sigma_{\Delta t} \) RMS variation of the input time error.
\( \sigma_{\Delta t,tdc} \) RMS variation of the time error induced by the TDC.
\( \sigma_\phi \) RMS variation of the input phase noise.
\( \sigma_{n,ims}, \sigma_{n,pre} \) RMS variation of the calibration loop noise.
Symbols

\( \sigma_h \)  
RMS variation of the LMS gain.

\( \sigma_{h_i}, \sigma_{g_i} \)  
RMS variation of the pre-distortion gains.

\( \sigma_w \)  
RMS variation of \( w \).
## Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog/Digital Converter.</td>
</tr>
<tr>
<td>ADPLL</td>
<td>All Digital Phase Locked Loop.</td>
</tr>
<tr>
<td>BB</td>
<td>Bang Bang.</td>
</tr>
<tr>
<td>CML</td>
<td>Current Mode Logic.</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor.</td>
</tr>
<tr>
<td>CDR</td>
<td>Clock and Data Recovery.</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital/Analog Converter.</td>
</tr>
<tr>
<td>DCO</td>
<td>Digitally Controlled Oscillator.</td>
</tr>
<tr>
<td>DEM</td>
<td>Dynamic Element Matching.</td>
</tr>
<tr>
<td>DLL</td>
<td>Delay-Locked Loop.</td>
</tr>
<tr>
<td>DTC</td>
<td>Digital/Time Converter.</td>
</tr>
<tr>
<td>DSMn</td>
<td>n-order Delta Sigma Modulator.</td>
</tr>
<tr>
<td>EFM</td>
<td>Error Feedback Model.</td>
</tr>
<tr>
<td>FoM</td>
<td>Figure of Merit.</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite Impulse Response.</td>
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<tr>
<td>GRO</td>
<td>Gated Ring Oscillator.</td>
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<tr>
<td>INL</td>
<td>Integral Non-Linearity.</td>
</tr>
<tr>
<td>LMS</td>
<td>Least Mean Square.</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator.</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit.</td>
</tr>
<tr>
<td>MASH</td>
<td>Multi-stAge noise SHaping.</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide Semiconductor Field-Effect Transistor.</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit.</td>
</tr>
<tr>
<td>PD</td>
<td>Phase Detector.</td>
</tr>
<tr>
<td>PI</td>
<td>Proportional Integral.</td>
</tr>
<tr>
<td>Phi</td>
<td>Phase Interpolator.</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop.</td>
</tr>
<tr>
<td>PSD</td>
<td>Power Spectra Density.</td>
</tr>
<tr>
<td>PVT</td>
<td>Power Voltage Process.</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency.</td>
</tr>
<tr>
<td>RHI5</td>
<td>Right Hand Side.</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square.</td>
</tr>
<tr>
<td>SFM</td>
<td>Signal Feedback Model.</td>
</tr>
<tr>
<td>TA</td>
<td>Time Amplifier.</td>
</tr>
<tr>
<td>TDC</td>
<td>Time/Digital Converter.</td>
</tr>
<tr>
<td>Acronym</td>
<td>Definition</td>
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<tr>
<td>TPD</td>
<td>Ternary Phase Detector.</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator.</td>
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</tbody>
</table>