

A Dissertation

**High Performance VLSI Architectures for QC-LDPC
Codes in 5G Communications**

submitted to

Department of Information and Communication Engineering

Graduate School

Inha University

in partial fulfillment of the requirements

for the degree of

Doctor of Philosophy

by

Nguyen Thi Bao Tram

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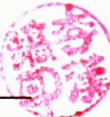
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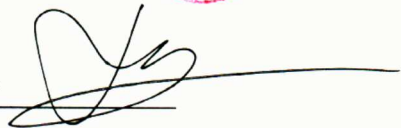
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Department of Information and Communication Engineering

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Abstract

The rapid development of electronic devices has brought about the advent of various emerging and future communication applications, which require significantly high throughput and low power budgets. The fifth-generation (5G) wireless communications system will enable the ever-advancing number of high-tech and Internet of Things (IoTs) devices to connect to the internet at incredibly higher speed and with lower latency. This is especially challenging for forward error correction (FEC) mechanisms in terms of hardware resources and energy since FEC decoding is one of the most computationally intensive processing blocks.

Low-density parity-check (LDPC) codes, which were first proposed by Gallager in the 1960s, attracted much attention due to their superior error-correction performance, and have been adopted as the channel coding scheme for 5G enhanced mobile broadband data channel in third generation partnership project (3GPP) standard meeting. The development of low-complexity and high-throughput LDPC decoder designs for 5G New Radio (NR) have necessitated a joint optimization of algorithms, architectures, and implementations to fulfill the growing demand for ever-increasing data rates.

This dissertation focuses on the design and implementation of various efficient very-large-scale integration architectures of quasi-cyclic low-density parity-check (QC-LDPC) codes for 5G NR communications. It aims at developing new approaches to the area and throughput optimizations while maintaining the required error correction performance of the LDPC codes. In this

work, a novel multi-way split-row layered LDPC decoding algorithm, which significantly reduces the hardware complexity by partitioning each decoding layer into multiple splits, is introduced. In addition, an efficient encoding method and a high-throughput low-complexity encoder architecture for QC-LDPC codes compliant with the 5G NR wireless communication standard is also described. The proposed encoder indicated a substantial reduction in the required area as well as memory storage when compared with existing state-of-the-art encoding approaches. The proposed encoder architecture is capable of supporting multiple code rates, various block lengths, and several different submatrix sizes. Generally, multi-mode architectures of QC-LDPC decoders for 5G NR wireless communication standard suffer from very complex routing and sorting networks since it caters various submatrix sizes. A novel multi-size circular-shift network structure for 5G NR QC-LDPC decoders is proposed. The proposed switch network is able to support all 51 different submatrix sizes as defined in 5G NR wireless communication standard through an efficient forward-routing switch network and enhance the hardware complexity using a cyclic shift size decomposition method. Moreover, a hardware-efficient QC-LDPC decoder architecture was implemented, in order to satisfy the strict latency and area constraints, imposed by the 5G NR wireless communication standards. By deploying the hardware reuse technique in check node passed processors, the proposed decoder outperforms its predecessors in terms of hardware complexity and throughput.

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Table of Contents

Abstract	i
Acknowledgements	iii
Table of Contents	iv
List of Figures	viii
List of Tables	xi
Glossary	xiii
1 Introduction	1
1.1 Overview	1
1.2 Contributions	4
1.3 Dissertation Organization	6
1.4 Publication List	8
2 Background and Fundamentals	10
2.1 Introduction	10
2.2 Digital Communications	10
2.3 Channel Coding	12
2.4 Introduction of LDPC codes	14

2.5	Quasi-Cyclic LDPC Codes	17
2.6	LDPC Codes for 5G New Radio	19
2.6.1	Introduction	19
2.6.2	5G New Radio QC-LDPC Characteristics	20
2.7	LDPC Encoding	25
2.7.1	LDPC Encoding with Gaussian Elinination	25
2.7.2	LDPC Encoding with Richardson-Urbanke Method	26
2.8	LDPC Decoding	30
2.8.1	Message-Passing Decoding Algorithm	30
2.8.2	Hard Decision Bit-Flipping Algorithm	33
2.8.3	Soft Decision Belief Propagation Algorithm	34
2.8.4	Modified Min-Sum Algorithm	42
2.9	LDPC Scheduling	45
2.9.1	Flooding Decoding Algorithm	46
2.9.2	Layered Decoding Algorithm	46
2.9.3	Pipelined Layered Decoding Algorithm	50
2.10	Summary	52
3	Low-Complexity Multi-Way Split-Row Layered LDPC Decoder for Gigabit Wireless Communications	53
3.1	Introduction	53
3.2	Proposed Multi-Way Split-Row Layered LDPC Decoding Algo- rithm	54
3.3	Proposed Multi-Way Split-Row Layered LDPC Decoder Archi- tecture	56

3.4	Implementation Results and Comparison	64
3.5	Summary	70
4	Efficient QC-LDPC Encoder for 5G New Radio	71
4.1	Introduction	71
4.2	Proposed 5G New Radio QC-LDPC Encoder Design	72
4.2.1	Proposed QC-LDPC Encoding Algorithm	72
4.2.2	Proposed QC-LDPC Encoder Architecture	78
4.3	Implementation Results and Comparison	81
4.4	Summary	84
5	Low-Complexity Multi-Size Circular-Shift Network for 5G New Radio QC-LDPC Decoders	86
5.1	Introduction	86
5.2	Multi-Size Circular-Shift Network for LDPC Decoder	87
5.3	Proposed Low-Complexity Multi-Size Circular-Shift Network for 5G New Radio LDPC Decoder	93
5.3.1	Modified Lifting Size Table for 5G New Radio LDPC Codes	93
5.3.2	Structure of Forward Routing Network	94
5.3.3	Fine-Coarse Structure for Circular-Shift Network	96
5.3.4	Proposed Low-Complexity Multi-Size Circular-Shift Net- work	98
5.4	Implementation Results and Comparison	102
5.5	Summary	103

6	Low-Complexity High-Throughput QC-LDPC Decoder for 5G	
	New Radio	104
6.1	Introduction	104
6.2	Combined Min-Sum Algorithm	107
6.3	Proposed LDPC Decoder Architecture	109
6.3.1	Overall Decoder Architecture	110
6.3.2	Memory Blocks	111
6.3.3	Switch Network	113
6.3.4	Variable Node Units	113
6.3.5	Check Node Units	115
6.3.6	A Posteriori Information Update Units	119
6.3.7	Controller Block	120
6.4	Implementation Results and Comparison	121
6.5	Summary	125
7	Conclusions and Future Work	126
7.1	Conclusions	126
7.2	Future Work	128
	Bibliography	130

List of Figures

2.1	Block diagram of a digital communication system.	11
2.2	Generic channel coding system.	12
2.3	Sample (a) H -Matrix and (b) Tanner graph.	14
2.4	Sketch of base parity-check structure for the 5G NR QC-LDPC codes.	21
2.5	Shortening by zero padding and puncturing of standard 5G QC-LDPC codes.	24
2.6	The parity-check matrix H in approximate lower triangular form.	27
2.7	Flow diagram of an iterative message-passing decoding algorithm.	31
2.8	Flooding decoding schedule for the LDPC decoding algorithms.	47
2.9	Layered decoding schedule for the LDPC decoding algorithms. .	49
3.1	H -matrix splits for code rate $3/4$ of IEEE 802.11ad (a) $s = 2$; (b) $s = 4$	55
3.2	Proposed s -way splitting layered LDPC decoder.	58
3.3	Proposed multi-way split-row pipelined layered LDPC decoder ($s = 2$).	60

3.4	Pipelined schedule for proposed multi-way split-row pipelined layered LDPC decoder ($s = 2$).	64
3.5	FER performance of IEEE 802.11ad LDPC code for four supported code rates with different levels of splitting at five-bit quantization.	65
4.1	Low-complexity high-throughput encoder architecture for 5G NR QC-LDPC code.	78
5.1	(a) Benes network 2×2 switch; (b) Benes network when $P = 8$; (c) Banyan network when $P = 8$	88
5.2	(a) RIP structure; (b) RIS structure.	90
5.3	Pre-rotator and MUX-network structure.	92
5.4	(a) Lifting size Z table; (b) Modified lifting size Z table for standard 5G LDPC codes.	94
5.5	Forward Routing Circular-Shift Network Structure.	95
5.6	Fine-coarse structure.	96
5.7	Proposed MSCS network structure for 5G NR LDPC decoders.	99
6.1	Schematic representation of base matrix BG1 defined by 5G NR standard for generating a QC-LDPC code of codelength $N = 3808$ bits, code-rate $R = 1/3$, and $Z = 56$	106
6.2	Proposed overall low-complexity high-throughput pipelined layered QC-LDPC decoder architecture.	112
6.3	Proposed variable node update unit architecture.	114

6.4	Check-to-variable node message in decompressed and compressed format.	115
6.5	Proposed check node update unit architecture.	117
6.6	Architecture of 2^k -FMVG unit using the TS approach.	118
6.7	Proposed a posteriori information update unit architecture. . .	120
6.8	Decoding performance of the QC-LDPC decoders on the $N =$ 3808 , $R = 1/3$ for BG1 base matrix of 5G NR wireless commu- nication standard.	121

List of Tables

2.1	Relationship between exponent matrices and sets of lifting size.	22
2.2	Lifting size Z supported by standard 5G QC-LDPC codes.	24
2.3	Complexity analysis of p_1^T calculation.	29
2.4	Complexity analysis of p_2^T calculation.	30
3.1	Area breakdown per sub-block of the proposed LDPC decoder.	66
3.2	Hardware complexity comparison for LDPC decoders.	67
3.3	Implementation results and performance comparison of the proposed LDPC decoder.	69
4.1	Comparison between Gaussian method, RU method, and proposed method.	82
4.2	Comparison between Gaussian method, RU method, and proposed method for submatrix size $Z = 16$	83
4.3	ASIC implementation results of LDPC encoders for different lifting sizes $Z = 30, 64, 96, 144,$ and 352	85
5.1	ASIC Implementation Results of Multi-Size Circular-Shift Network for 5G NR LDPC Decoders.	102

6.1	Check node degree d_c distribution for 5G NR LDPC codes. . .	107
6.2	Components required for the minimum finders of $d_c = 19$ inputs of bit-width $(w - 1)$	118
6.3	Implementation and comparison for 5G QC-LDPC decoders. . .	123

Glossary

3GPP Third Generation Partnership Project

5G Fifth-Generation

ALT Approximate Lower Triangular

ASIC Application-Specific Integrated Circuit

AWGN Additive White Gaussian Noise

BER Bit Error Rate

BF Bit Flipping

BP Belief Propagation

BPSK Binary Phase-Shift Keying

CMOS Complimentary Metal Oxide Semiconductor

CNBP Check Node-Based Processor

CNU Check Node Unit

eMBB Enhanced Mobile Broadband

FEC Forward Error Correction

FER Frame Error Rate

FMVG First Minimum Value Generator

FRCS Forward Routing Circular-Shift

GCD Greatest Common Divisor

IEEE Institute of Electrical and Electronics Engineers

IMWBF Improved Modified Weighted Bit Flipping

IoT Internet of Things

IR-HARQ Incremental Redundancy Hybrid Automatic Repeat Request

ITU-R International Telecommunication Union - Radiocommunication Sector

LDPC Low-Density Parity-Check

LLR Log-Likelihood Ratio

LUT Look-Up Table

ML Maximum Likelihood

mMTC Massive Machine Type Communications

mmWave millimeter Wave

MWBF Modified Weighted Bit Flipping

MPA Message Passing Algorithm

MS Min-Sum

MSCS Multi-size Circular-Shift

MUX Multiplexer

NR New Radio

OMS Offset Min-Sum

QC Quasi-Cyclic

RAM Random-Access Memory

RIP Rotator-In-Parallel

RIS Rotator-In-Series

ROM Read-Only Memory

RU Richardson-Urbanke

SNR Signal-to-Noise Ratio

SMARTER Study on New Services and Markets Technology Enablers

SPA Sum-Product Algorithm

SPC Single Parity-Check

TAR Throughput-to-Area Ratio

TS Tree Structure

TSMC Taiwan Semiconductor Manufacturing Company

URLLC Ultra Reliable Low Latency Communications

VLSI Very-Large-Scale Integration

VNU Variable Node Unit

WBF Weighted Bit Flipping

WiGig Wireless Gigabit

WiMAX Worldwide Interoperability for Microwave Access

WPAN Wireless Personal Area Network