A Dissertation

High Performance VLSI Architectures for QC-LDPC Codes in 5G Communications

submitted to

Department of Information and Communication Engineering

Graduate School

Inha University

in partial fulfillment of the requirements

for the degree of

Doctor of Philosophy

by

Nguyen Thi Bao Tram

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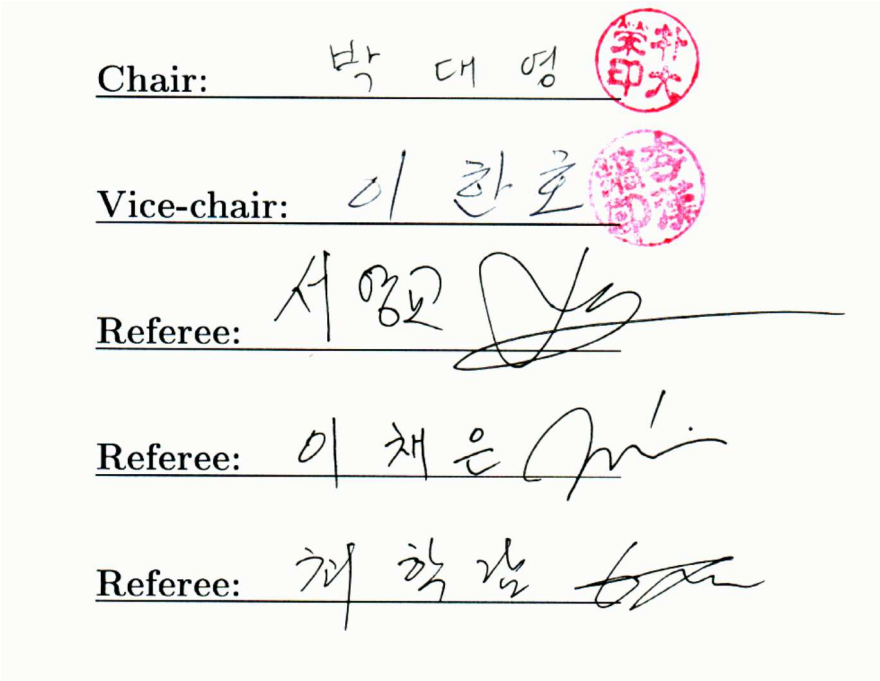
Major: Information and Communication Engineering

Advisor: Professor Hanho Lee

This certifies that the dissertation of Nguyen Thi Bao Tram is approved



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Abstract

The rapid development of electronic devices has brought about the advent of various emerging and future communication applications, which require significantly high throughput and low power budgets. The fifth-generation (5G) wireless communications system will enable the ever-advancing number of high-tech and Internet of Things (IoTs) devices to connect to the internet at incredibly higher speed and with lower latency. This is especially challenging for forward error correction (FEC) mechanisms in terms of hardware resources and energy since FEC decoding is one of the most computationally intensive processing blocks.

Low-density parity-check (LDPC) codes, which were first proposed by Gallager in the 1960s, attracted much attention due to their superior error-correction performance, and have been adopted as the channel coding scheme for 5G enhanced mobile broadband data channel in third generation partnership project (3GPP) standard meeting. The development of low-complexity and high-throughput LDPC decoder designs for 5G New Radio (NR) have necessitated a joint optimization of algorithms, architectures, and implementations to fulfill the growing demand for ever-increasing data rates.

This dissertation focuses on the design and implementation of various efficient very-large-scale integration architectures of quasi-cyclic low-density parity-check (QC-LDPC) codes for 5G NR communications. It aims at developing new approaches to the area and throughput optimizations while maintaining the required error correction performance of the LDPC codes. In this

work, a novel multi-way split-row layered LDPC decoding algorithm, which significantly reduces the hardware complexity by partitioning each decoding layer into multiple splits, is introduced. In addition, an efficient encoding method and a high-throughput low-complexity encoder architecture for QC-LDPC codes compliant with the 5G NR wireless communication standard is also described. The proposed encoder indicated a substantial reduction in the required area as well as memory storage when compared with existing state-of-the-art encoding approaches. The proposed encoder architecture is capable of supporting multiple code rates, various block lengths, and several different submatrix sizes. Generally, multi-mode architectures of QC-LDPC decoders for 5G NR wireless communication standard suffer from very complex routing and sorting networks since it caters various submatrix sizes. A novel multi-size circular-shift network structure for 5G NR QC-LDPC decoders is proposed. The proposed switch network is able to support all 51 different submatrix sizes as defined in 5G NR wireless communication standard through an efficient forward-routing switch network and enhance the hardware complexity using a cyclic shift size decomposition method. Moreover, a hardware-efficient QC-LDPC decoder architecture was implemented, in order to satisfy the strict latency and area constraints, imposed by the 5G NR wireless communication standards. By deploying the hardware reuse technique in check node passed processors, the proposed decoder outperforms its predecessors in terms of hardware complexity and throughput.

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Table of Contents

List of Figures

List of Tables

Glossary

3GPP Third Generation Partnership Project

5G Fifth-Generation

ALT Approximate Lower Triangular

ASIC Application-Specific Integrated Circuit

AWGN Additive White Gaussian Noise

BER Bit Error Rate

BF Bit Flipping

BP Belief Propagation

BPSK Binary Phase-Shift Keying

CMOS Complimentary Metal Oxide Semiconductor

CNBP Check Node-Based Processor

CNU Check Node Unit

eMBB Enhanced Mobile Broadband

FEC Forward Error Correction

FER Frame Error Rate

FMVG First Minimum Value Generator

FRCS Forward Routing Circular-Shift

GCD Greatest Common Divisor

IEEE Institute of Electrical and Electronics Engineers

IMWBF Improved Modified Weighted Bit Flipping

IoT Internet of Things

IR-HARQ Incremental Redundancy Hybrid Automatic Repeat Request

ITU-R International Telecommunication Union - Radiocommunication Sector

LDPC Low-Density Parity-Check

LLR Log-Likelihood Ratio

LUT Look-Up Table

ML Maximum Likelihood

mMTC Massive Machine Type Communications

mmWave milimeter Wave

MWBF Modified Weighted Bit Flipping

MPA Message Passing Algorithm

MS Min-Sum

MSCS Multi-size Circular-Shift

MUX Multiplexer

NR New Radio

OMS Offset Min-Sum

QC Quasi-Cyclic

RAM Random-Access Memory

RIP Rotator-In-Parallel

RIS Rotator-In-Series

ROM Read-Only Memory

RU Richardson-Urbanke

SNR Signal-to-Noise Ratio

SMARTER Study on New Services and Markets Technology Enablers

SPA Sum-Product Algorithm

SPC Single Parity-Check

TAR Throughput-to-Area Ratio

TS Tree Structure

TSMC Taiwan Semiconductor Manufacturing Company

URLLC Ultra Reliable Low Latency Communications

VLSI Very-Large-Scale Integration

VNU Variable Node Unit

WBF Weighted Bit Flipping

WiGig Wireless Gigabit

WiMAX Worldwide Interoperability for Microwave Access

WPAN Wireless Personal Area Network